WHAT IS CLAIMED IS:

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1. A method for executing a set of instructions in a processor, comprising:

decoding the set of instructions; and

steering each of the set of instructions into an instruction cache according to a particular one of a set of execution units that the instruction requires.

2. The method of claim 1 further comprising storing each of the set of instructions into a particular one of a set of bins in the instruction cache that corresponds to the particular one of the set of execution units that the instruction requires.

3. The method of claim 1 further comprising renaming a set of registers of a particular one of the set of instructions, prior to steering the set of instructions into the instruction cache.

4. The method of claim 3 further comprising scheduling a particular one of the set of instructions if the particular one of the set of instructions is found in the instruction cache.

5. The method of claim 4 further comprising executing the particular one of the set of instructions that is scheduled, using the particular one of the set of execution units that the particular one of the set of instructions requires.

6. The method of claim 3 further comprising fetching a particular one of the set of instructions from a memory device if the particular one of the set of instructions is not found in the instruction cache.

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7. A method for executing a set of instructions in a processor, comprising:

decoding the set of instructions;

scheduling the set of instructions to avoid pipeline stalls; and

steering each of the set of instructions into an instruction cache according to a particular one of a set of execution units that the instruction requires.

8. The method of claim 7 further comprising storing each of the set of instructions into a particular one of a set of bins in the instruction cache that corresponds to the particular one of the set of execution units that the instruction requires.

9. The method of claim 7 further comprising renaming a set of registers of a particular one of the set of instructions, prior to scheduling the set of instructions.

10. The method of claim 9 further comprising executing the particular one of the set of instructions, using the particular one of the set of execution units that the instruction requires, if the particular one of the set of instructions is found in the instruction cache.

11. The method of claim 9 further comprising fetching a particular one of the set of instructions from a memory device if the particular one of the set of instructions is not found in the instruction cache.

12. A method for executing a set of instructions in a processor, comprising:

decoding the set of instructions; and

steering a first time each of the set of instructions into an instruction cache according to a particular one of a set of execution unit clusters that the instruction requires.

13. The method of claim 12 further comprising storing each of the set of instructions into a particular one of a set of bins in the instruction cache that corresponds to the particular one of the set of execution unit clusters that the instruction requires.

14. The method of claim 12 further comprising renaming a set of registers of a particular one of the set of instructions, prior to steering the set of instructions into the instruction cache.

15. The method of claim 14 further comprising scheduling a particular one of the set of instructions if the particular one of the set of instructions is found in the instruction cache.

16. The method of claim 15 further comprising steering, at a second time, the particular one of the set of instructions that is scheduled into one of a set of execution units, within the particular one of the set of execution unit clusters, that the instruction requires.

17. The method of claim 16 further comprising executing the particular one of the set of instructions that is steered the second time, using the one of the set of execution units that the particular one of the set of instructions requires.

18. The method of claim 14 further comprising fetching a particular one of the set of instructions from a memory device if the particular one of the set of instructions is not found in the instruction cache.

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19. A processor, comprising:

an instruction cache; and

a crossbar, coupled to the instruction cache, to steer each of a set of instructions into the instruction cache according to a particular one of a set of execution units that the instruction requires.

20. The processor of claim 19 wherein the instruction cache includes a set of bins, each of the set of bins corresponding to a particular one of a set of execution units that a particular one of the set of instructions requires.

21. The processor of claim 19 further comprising a register renaming unit, coupled to the crossbar, to eliminate false data dependencies.

22. The processor of claim 21 further comprising a set of reservation stations, each of the set of reservation stations coupled to a corresponding one of the set of bins in the instruction cache, to schedule the set of instructions to avoid pipeline stalls.

23. The processor of claim 21 further comprising a reservation station, coupled to the register renaming unit, to schedule the set of instructions to avoid pipeline stalls.

24. A processor, comprising:

an instruction cache; and

a first crossbar, coupled to the instruction cache, to steer each of a set of instructions into the instruction cache according to a particular one of a set of execution unit clusters that the instruction requires.

25. The processor of claim 24 wherein the instruction cache includes a set of bins, each of the set of bins corresponding to a particular one of a set of execution unit clusters that a particular one of the set of instructions requires.

26. The processor of claim 24 further comprising a register renaming unit, coupled to the first crossbar, to eliminate false data dependencies.

27. The processor of claim 26 further comprising a set of reservation stations, each of the set of reservation stations coupled to a corresponding one of the set of bins in the instruction cache, to schedule the set of instructions to avoid pipeline stalls.

28. The processor of claim 27 further comprising a set of second crossbars, each of the set of second crossbars coupled to a corresponding one of the set of reservation stations, to steer, at a second time, each of the set of instructions to a particular one of a set of execution units, within the particular one of the set of execution unit clusters, that the instruction requires.